2

Noise in Analog and Digital Systems

Erik A. McShane and
Krishna Shenai
Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, Illinois, USA

2.1 Introduction 101
2.2 Analog (Small-Signal) Noise 101
2.2.1 Noise Categories • 2.2.2 White Noise • 2.2.3 Pink Noise
2.3 Digital (Large-Signal) Noise 105
2.3.1 Noise Categories • 2.3.2 Series Resistance • 2.3.3 Dynamic Charge Sharing
2.3.4 Noise Margins
Bibliography 108

2.1 Introduction

Noise from an analog (or **small-signal**) perspective is a random time-varying signal that is generated in all passive and active electronic devices. It can be represented as either a current or a voltage, $i_n(t)$ or $v_n(t)$. Over a fixed time period, t, the average value of noise is zero. Analog noise, therefore, is commonly presented in terms of its **mean-square** value (I_{rms}^2 or V_{rms}^2). It is sometimes also described by its **root-mean-square** value (I_{rms} or V_{rms}).

Noise in digital (or **large-signal**) circuits is the perturbation of one nonlinear signal, the **noise victim**, by a second nonlinear signal, the **noise aggressor**. The perturbation is introduced by a parasitic coupling path that is resistive, capacitive, or inductive in nature. Since digital systems are typically characterized by voltage levels, digital noise is presented in terms of voltage and voltage transients, $v_n(t)$ and dv_n/dt.

The impact of noise differs for analog and digital systems and leads to unique equivalent circuit models and analytical techniques. Analog noise is treated by linearized expressions that correspond to small-signal equivalent circuit parameters. Digital noise is analyzed by large-signal expressions that define logic transitions. In this chapter, the characteristics of noise are presented for both systems. Several examples are included for each type of system.

For further reading, several respected books are listed in the Bibliography section of this chapter. These provide a more thorough background on analog and digital systems, network theory, and the introduction of noise to classical systems analysis.

2.2 Analog (Small-Signal) Noise

Noise in analog systems is typically characterized by its impact as a small-signal perturbation. In this form, noise is considered to be an independent alternating current (ac) source (either voltage or current). Table 2.1 lists the nomenclature for discussing analog noise. These measures are derived and defined throughout the chapter.

The relationships as a function of time for noise voltage, square noise voltage, and mean-square noise voltage are illustrated in Figure 2.1; similar waveforms can also be shown for representating noise current. If multiple noise sources are present, they are considered to be independent and uncorrelated. Therefore, the cumulative noise contribution can be expressed in mean-square units by:

$$\overline{i_n^2} = \overline{i_{n1}^2} + \overline{i_{n2}^2}, \tag{2.1}$$

as the sum of the individual mean-square components. In *rms* terms, the total noise is represented by:

$$i_{n,\,rms} = \sqrt{i_{n1,\,rms}^2 + i_{n2,\,rms}^2}. \tag{2.2}$$

TABLE 2.1 Nomenclature in Analog (Small-Signal) Noise Analysis

Name	Current-referred symbol	Units	Voltage-referred symbol	Units
Noise signal	$i_n(t)$	A	$v_n(t)$	V
Mean-square noise signal	$\overline{i_n^2(t)}$	A^2_{rms}	$\overline{v_n^2(t)}$	V^2_{rms}
Root-mean-square noise signal	$\sqrt{\overline{i_n^2(t)}}$ or $i_{n,\,rms}$	A_{rms}	$\sqrt{\overline{v_n^2(t)}}$ or $v_{n,\,rms}$	V_{rms}
Noise power spectral density	$S_I(f)$	A^2/Hz	$S_V(f)$	V^2/Hz
Root noise power spectral density	$\sqrt{S_I(f)}$	$A/\sqrt{Hz}$	$\sqrt{S_V(f)}$	$V/\sqrt{Hz}$

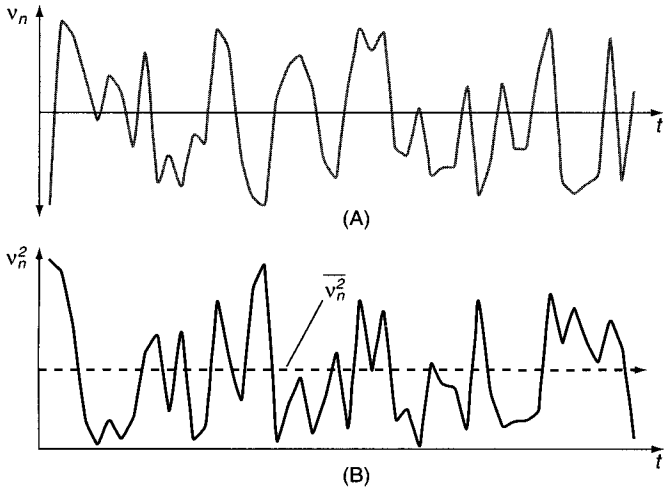

FIGURE 2.1

Some noise also exhibits a frequency dependence. If the noise mean-square value of spectral components in a narrow bandwidth (Δf) is determined, then the ratio of that value to Δf is defined as the **noise power spectral density** (the noise **mean-square per bandwidth**). Mathematically, the definition is expressed in terms of noise current as:

$$S_I(f) = \lim_{\Delta f \to 0} \frac{\overline{i_n^2(t)}}{\Delta f}. \tag{2.3}$$

The relationship can be reversed to define the mean-square noise current in terms of the noise power spectral density by:

$$\overline{i_n^2} = \int_{f_1}^{f_2} S_I(f)df. \tag{2.4}$$

Equivalent expressions can be derived for $S_V(f)$, the noise power in terms of noise voltage.

2.2.1 Noise Categories

Analog small-signal noise can be subdivided into two categories: frequency independent (or **white**) noise and frequency dependent (or **pink**) noise. The spectrum of the former is constant to frequencies as high as 10^{14} Hz. In the latter, the noise power is a function of $1/f^n$, where typically $n = 1$ (although some forms of noise obey a power relationship with $n \geq 2$). The total noise power in an element, as shown in Figure 2.2, is the combination of both, and a clear knee frequency is observed. The terms S_{Iw} and S_{Ip} are used to refer to the specific contributions of white and pink noise, respectively, to the total noise power.

Table 2.2 lists the common characteristics of small-signal noise. The expressions are developed more fully in the following subsections.

2.2.2 White Noise

White noise sources are composed of **thermal** (also called **Johnson** or **Nyquist**) noise and **shot** noise. Thermal noise is generated by all resistive elements and is associated with the random motion of carriers in an electronic element. It is a function only of temperature. Shot noise is associated with the discretization of charged particles and is always present in semiconductor *pn* junctions. It is a function only of dc current flow.

The thermal noise of a resistance, R, can be modeled as an ideal resistor and an independent current or voltage source, as shown in Figure 2.3. The Thevenin equivalent noise voltage is given by:

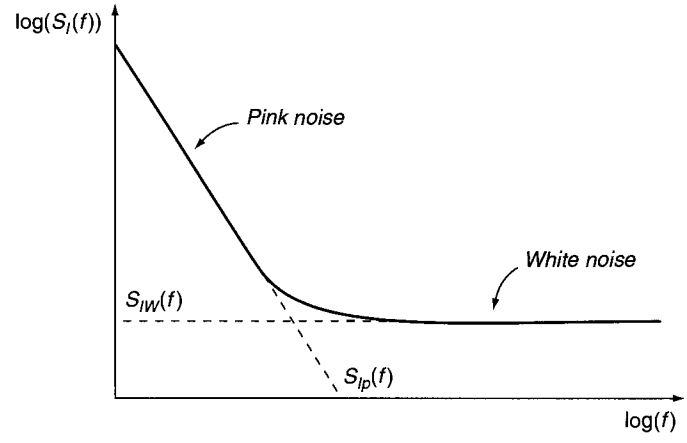

FIGURE 2.2

TABLE 2.2 Characteristics of Analog (Small-Signal) Noise

Name	Type	Dependence	Expression
Thermal (or Johnson or Nyquist)	White	Temperature	$\overline{v_n^2} = 4\hat{k}TR\Delta f$
Shot	White	Current	$\overline{i_n^2} = 2qI\Delta f$
Capacitor bandwidth-limited	White	Temperature, bandwidth	$v_{n,\text{rms}} = \sqrt{\frac{\hat{k}T}{C}}$
Inductor bandwidth-limited	White	Temperature, bandwidth	$i_{n,\text{rms}} = \sqrt{\frac{\hat{k}T}{L}}$
Flicker (or $1/f$)	Pink	Current	$\overline{v_n^2} = K_R \frac{R_{sq}^2}{A} V^2 \frac{\Delta f}{f}$
			$\overline{i_n^2} = \frac{K_D I}{A} \frac{\Delta f}{f}$
			$\overline{v_{n,\text{eq}}^2} = \frac{K_M}{WLC_{ox}^2} \frac{\Delta f}{f}$
Popcorn	Pink	Recombination	$\propto \frac{1}{f^2}$

Constants:

$\hat{k} = 1.38 \times 10^{-23}\ \text{V} \cdot \text{C/K}$

$q = 1.6 \times 10^{-19}\ \text{C}$

$K_R \approx 5 \times 10^{-24}\ \text{cm}^2/\Omega^2$

$K_D \approx 10^{-21}\ \text{cm}^2 \cdot \text{A}$

$K_M \approx \begin{cases} 10^{-33}\text{C}^2/\text{cm}^2(p\text{JFET}) \\ 10^{-32}\text{C}^2/\text{cm}^2(\text{PMOSFET}) \\ 4 \times 10^{-31}\text{C}^2/\text{cm}^2(\text{NMOSFET}) \end{cases}$

$$\overline{v_n^2} = 4\hat{k}TR\Delta f, \tag{2.5}$$

where $\hat{k}$ is Boltzmann's constant ($1.38 \times 10^{-23}\ \text{V} \cdot \text{C/K}$), T is absolute temperature (in degrees Kelvin), and Δf is the noise bandwidth. The Norton equivalent noise current can also be obtained. It is expressed as:

$$\overline{i_n^2} = 4\hat{k}T\frac{1}{R}\Delta f. \tag{2.6}$$

A MOSFET's channel resistance also produces a thermal noise current according to equation 2.6. Since it is informative to compare the MOSFET noise current with the small-signal input stimulus, the output noise current can be referred back to the source using the amplifier gain expression:

$$i_d = g_m v_{gs}, \tag{2.7}$$

such that the equivalent input noise voltage is as follows:

$$\overline{v_{n,\text{eq}}^2} = \frac{4\hat{k}T}{Rg_m^2}\Delta f. \tag{2.8}$$

In the saturation regime, the channel resistance can be approximated by $1/g_m$, and the channel pinch-off reduces the effective noise to about 66% of its nominal value. Therefore, equation 2.8 can be simplified to:

$$\overline{v_{n,\text{eq}}^2} = \frac{8\hat{k}T}{3}\frac{1}{g_m}\Delta f. \tag{2.9}$$

Both MOSFET channel thermal noise source configurations are shown in Figure 2.4. It should be noted that the input noise voltage representation is valid only at low frequencies. As the frequency rises, the admittance of gate parasitic capacitances (C_{GD} and C_{GS}) becomes higher; $\overline{v_{n,\text{eq}}^2}$ is dropped partly on the gate impedance and partly on the output resistance of the

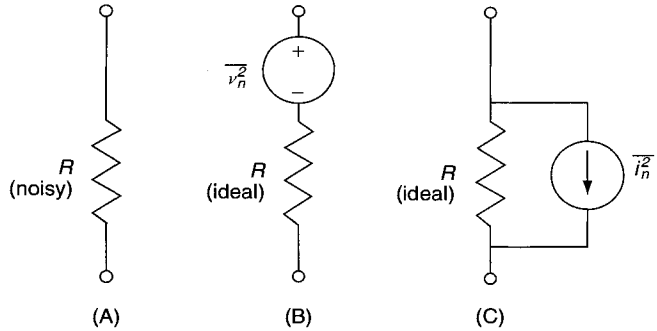

FIGURE 2.3

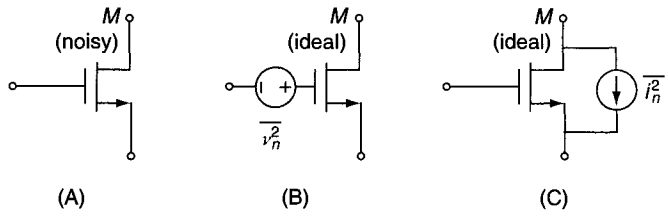

FIGURE 2.4

preceding device. Therefore, the ideal noiseless MOSFET is stimulated by an erroneously low noise voltage, resulting in inaccurate predictions of output noise.

Likewise, the shot noise of a junction diode, *D*, can be modeled as an ideal diode and an independent current source, as shown in Figure 2.5. The Norton equivalent noise current is given by

$$\overline{i_n^2} = 2qI\Delta f, \tag{2.10}$$

where I is the dc current conducted by the diode and Δf is the noise bandwidth. Noise is generated by the junction in both forward- and reverse-biased conditions since either a forward current or a leakage current is present.

Many analog circuits such as filters, sample-and-hold amplifiers, and switched-capacitor networks employ a resistor or a conductance that is bandwidth-limited by a capacitance or inductance. Just as the reactance of the inductor or capacitor limits the bandwidth of the input signal, it also affects the noise bandwidth. In the case of an RC circuit, the *rms* noise voltage is expressed as:

$$v_{n,\,rms} = \sqrt{\frac{\hat{k}T}{C}}. \tag{2.11}$$

A complementary result can be obtained for RL circuits, with the *rms* noise current expressed as:

$$i_{n,\,rms} = \sqrt{\frac{\hat{k}T}{L}}. \tag{2.12}$$

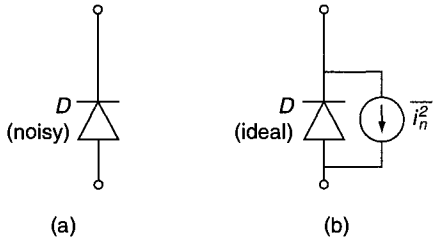

FIGURE 2.5

The expressions of equations 2.11 and 2.12 are interesting in that the resulting noise voltage or current is independent of the resistance or conductance. The total noise can be reduced only by choosing larger values for the reactive elements.

2.2.3 Pink Noise

Pink noise sources consist of **flicker** (also called $1/f$) **noise** and **popcorn noise**. Flicker noise pertains to the conductive properties of an electronic element. Other theories attribute flicker noise to interface traps present at oxide-semiconductor interfaces or to fluctuations in mobility. The noise is a function of the material homogeneity, its volume, the current, and the frequency. Popcorn noise, on the other hand, is proportional to $1/f^2$ and is an indication of poor semiconductor manufacturing. It is associated with distinct recombination processes and appears as a series of low-frequency noise bursts. Because it is uncommon, popcorn noise is not discussed further.

Flicker noise is proportional to current and inversely proportional to volume. Since electronic devices are three-dimensional structures, planar resistors and semiconductor junctions have unique expressions and scaling factors. For example, the flicker noise voltage of a resistor, *R*, is given as:

$$\overline{v_n^2} = K_R \frac{R_{sq}^2}{A} V^2 \frac{\Delta f}{f}, \tag{2.13}$$

where R_{sq} is the sheet resistance, A is the planar area of the resistor, V is the dc voltage, and K_R is a technology scaling constant ($\approx 5 \times 10^{-24}\,\text{cm}^2/\Omega^2$). The flicker noise current of a junction diode is similarly found as:

$$\overline{i_n^2} = \frac{K_D I}{A} \frac{\Delta f}{f}, \tag{2.14}$$

where A is the cross-sectional area of the diode, I is the dc current, and K_D is a diode scaling constant ($\approx 10^{-21}\,\text{cm}^2 \cdot \text{Å}$).

Finally, the input referred flicker noise voltage in a MOSFET is found by an expression that is derived from equation 2.14. It is given by:

$$\overline{v_{n,\,eq}^2} = \frac{K_M}{WLC_{ox}^2} \frac{\Delta f}{f}, \tag{2.15}$$

where W and L are, respectively, the gate width and length, C_{ox} is the oxide capacitance per unit area, and technology constant K_M is found experimentally. Recent empirical values for three types of FET are:

p-type JFET	$\approx 10^{-33}\,\text{C}^2/\text{cm}^2$
PMOSFET	$\approx 10^{-32}\,\text{C}^2/\text{cm}^2$
NMOSFET	$\approx 4 \times 10^{-31}\,\text{C}^2/\text{cm}^2$

2.3 Digital (Large-Signal) Noise

Noise in digital systems is typically characterized by the integrity of the voltages that represent the logic 0 and logic 1 states. Noise can manifest itself either during switching (when it may result in switching times that exceed theoretical results) or in static conditions. Even in CMOS logic, which nominally provides fully rail-to-rail logic levels, dynamic noise events can momentarily perturb a voltage level. Deep submicron technologies, which typically employ supply voltages of under 1.8 V, may be especially susceptible to logic glitches or errors that are induced by random coupled noise.

Table 2.3 lists the nomenclature used for discussing digital noise. These terms are derived and defined throughout the chapter.

2.3.1 Noise Categories

Several categories of noise are present in digital circuits. These include **series resistance**, dynamic charge sharing of hard and soft nodes, and ***I/O* integrity**, which are the types discussed in this chapter. They can appear in any combination, but for simplicity, the analysis below considers each noise source independently. All are strongly dependent on the specifications of the semiconductor manufacturing process, the physical arrangement of gates and interconnections on an integrated circuit, the switching frequency, and the relative activity level of adjacent gates or interconnections.

Table 2.4 lists the fundamental characteristics of large-signal noise. The expressions derived below demonstrate the impact of noise on either the input logic level (V_{IL} or V_{IH}) or the output logic level (V_{OL} or V_{OH}). Through these four parameters, noise indirectly affects the low and high noise margins.

2.3.2 Series Resistance

The effect of **series resistance** is to degrade output voltage levels (push them away from the rails). Series resistance can be present in the supply rail and/or the ground rail. Each series resistance has a different effect on the output characteristics. Ground rail resistance degrades V_{OL} and supply rail resistance degrades V_{OH}.

For example, consider the CMOS inverter shown in Figure 2.6(A) that includes a ground resistance R_{series}. The output voltage, V_O, can be modeled [see Figure 2.6(B)] as a resistor–divider network such that:

$$V_O = \frac{R_{\text{NMOS}} + R_{\text{series}}}{R_{\text{NMOS}} + R_{\text{PMOS}} + R_{\text{series}}} Vdd, \tag{2.16}$$

where R_{NMOS} and R_{PMOS} are the output resistances of the inverter gates and R_{series} is the ground resistance. If the inverter input is a logic 1, the NMOS is strongly conducting and therefore $R_{\text{NMOS}} \approx 0$. Then equation 2.16 can be simplified to:

$$V_O = \frac{R_{\text{series}}}{R_{\text{PMOS}} + R_{\text{series}}} Vdd. \tag{2.17a}$$

The output voltage is increased by the presence of the series resistance. A complementary result can be obtained for a supply rail resistance and an input of logic 0, which yields:

TABLE 2.3 Nomenclature in Digital (Large-Signal) Noise Analysis

Name	Symbol	Units
Input low (highest voltage acceptable as a logic '0')	V_{IL}	V
Input high (lowest voltage acceptable as a logic '1')	V_{IH}	V
Output low (nominal voltage produced as a logic '0')	V_{OL}	V
Output high (nominal voltage produced as a logic '1')	V_{OH}	V
Low-level noise margin	NM_L	V
High-level noise margin	NM_H	V

TABLE 2.4 Characteristics of Digital (Large-Signal) Noise

Name	Expression (CMOS)	Expression (NMOS)
V_{OL}	0	$\frac{1}{k}\frac{V_{TD}^2}{2(Vdd - V_{TN})}$
V_{OH}	Vdd	Vdd
V_{IL}	$\frac{3Vdd + 3V_{TP} + 5V_{TN}}{8}$	$V_{TN} - \frac{V_{TD}}{\sqrt{k(1+k)}}$
V_{IH}	$\frac{5Vdd + 5V_{TP} + 3V_{TN}}{8}$	$V_{TN} - \frac{2V_{TD}}{\sqrt{3k}}$
NM_L	$V_{IL} - V_{OL}$	
NM_H	$V_{OH} - V_{IH}$	

$$V_O = \frac{R_{NMOS}}{R_{NMOS} + R_{series}} Vdd. \quad (2.17b)$$

Supply and ground rails are designed to have minimal resistance to alleviate such effects as series resistance. This is accomplished by using low resistivity materials, increasing the cross-sectional area of the conductors, using shorter interconnection lengths, and applying other techniques. Two conditions, however, may still produce large voltage deviations. One condition is high-current *I/O* buffers, and the second condition is simultaneous switching of many parallel gates. The latter situation is illustrated in Figure 2.6(C).

If n gates (inverters in this example) with a common series resistance simultaneously switch the expressions of equations 2.17a and 2.17b, they can be modified as:

$$V_O = \frac{nR_{series}}{R_{PMOS} + nR_{series}} Vdd. \quad (2.18a)$$

and

$$V_O = \frac{R_{NMOS}}{R_{NMOS} + nR_{series}} Vdd. \quad (2.18b)$$

The effect of simultaneous switching becomes more pronounced as device density on integrated circuits rises and die sizes also increase.

2.3.3 Dynamic Charge Sharing

The phenomenon of **dynamic charge sharing** occurs when two functionally unrelated nodes become coupled due to a capacitance or mutual inductance. Coupling appears between any two interconnected lines that are adjacent or that overlap. In general, noise coupling is proportional to the cross-sectional area that is shared by the two lines. Coupling is also proportional to frequency and inversely proportional to the separation. Therefore, as integrated circuits are scaled to smaller dimensions and operate at higher frequencies, the detrimental effects of charge sharing become more severe.

Until recently, coupling was exclusively capacitive in nature. As integrated circuits reach frequencies of 1 GHz and above, however, inductive coupling also becomes significant. Results in this chapter, though, are limited to conventional capacitive coupling.

Consider, as shown in Figure 2.7(A), the two nodes v_n (the **noise aggressor** or source) and v_v (the **noise victim**) that are coupled by a capacitor C_c. Node v_v is also tied to ground through a generic admittance Y. In digital circuits, v_v can be either a **floating node** (such as found in dynamic logic, pass transistor logic, or memory cells) or a **driven node** (such as found in static logic). The admittance Y is therefore equivalent to either a second coupling capacitance C_p (from the floating node to the ground plane) or a resistance r_a (representing the output impedance of the gate driving the node). Both cases are illustrated in Figure 2.7.

A floating node's change in voltage at v_v that is produced by a signal at v_n is expressed as:

$$v_v = \frac{v_n C_c}{C_c + c_p}. \quad (2.19)$$

Because c_p is usually just the input capacitance of a logic gate, it is very small. Any value of C_c can cause significant charge-sharing to occur. Active nodes are much less susceptible to disruption by noise coupling since the equivalent output resistance, r_a, of the driving gate may be large ($> 10\,k\Omega$). The noise coupled to the victim node is written as:

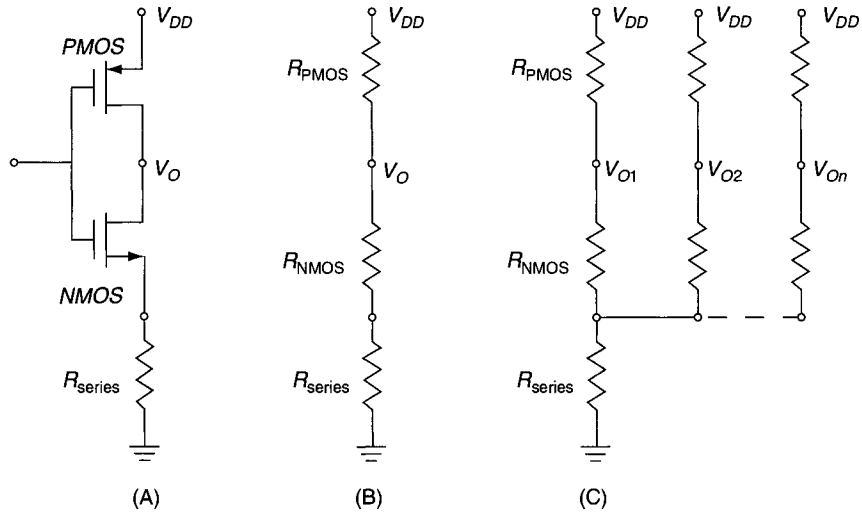

FIGURE 2.6

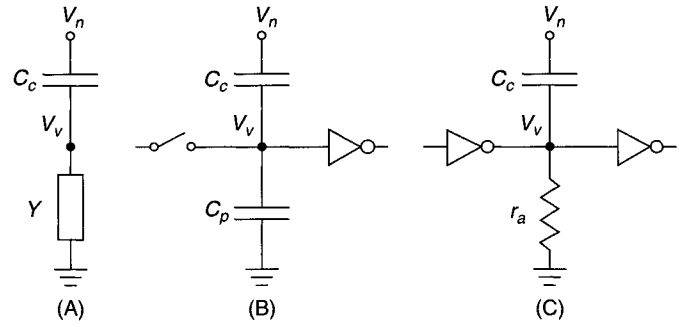

FIGURE 2.7

$$v_v = \frac{v_n r_a C_c s}{1 + r_a C_c s}. \tag{2.20}$$

Because typically $|r_a C_c s| \ll 1$, equation 2.20 can be reduced to:

$$v_v = v_n r_a C_c s. \tag{2.21}$$

Clearly for an actively driven node, a much larger coupling capacitance is necessary to produce a significant perturbation of the victim node.

2.3.4 Noise Margins

The *I/O* noise margins, NM_L and NM_H, refer to the ability of a logic gate to accommodate input noise without producing a faulty logic output. The input noise threshold levels, V_{IL} and V_{IH}, are by convention defined as the input voltages that result in a slope of -1 in the dV_O/dV_I response. This is shown in Figure 2.8. As is clear from Table 2.4, the noise margins of CMOS logic gates are larger than for comparable NMOS technologies. This is evident because CMOS delivers rail-to-rail outputs, whereas the V_{OL} is a circuit constraint in NMOS.

The noise margins of a CMOS gate can be found by first examining the dc transfer curve shown in Figure 2.8. From graphical analysis, the V_{IL} occurs when the PMOS is in its linear regime and the NMOS is in its saturation regime. Since a CMOS gate is complementary in operation, the V_{IH} by symmetry occurs when the PMOS is in its saturation regime and the NMOS is in its linear regime.

Considering first the CMOS V_{IL}, begin by equating the NMOS and PMOS currents:

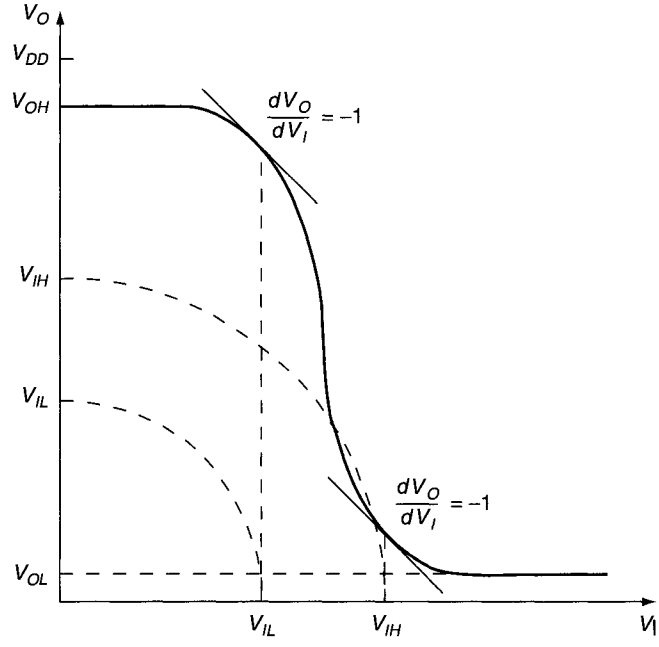

FIGURE 2.8

$$k_n \frac{W_n}{L_n} \frac{(V_I - V_{Tn})^2}{2} = k_p \frac{W_p}{L_p} \left(V_I - Vdd - V_{Tp} - \frac{V_O - Vdd}{2} \right) (V_O - Vdd). \tag{2.22}$$

Assuming that the inverter is designed to have a balanced transfer curve such that:

$$k_n \frac{W_n}{L_n} = k_p \frac{W_p}{L_p}, \tag{2.23}$$

then equation 2.22 reduces to a simpler form such that:

$$V_{IL} = \frac{3Vdd + 3V_{TP} + 5V_{TN}}{8}. \tag{2.24}$$

Considering next the CMOS V_{IH}, equating the NMOS and PMOS currents results in:

$$k_n \frac{W_n}{L_n} (V_I - V_{Tn} - \frac{V_O}{2}) V_O = k_p \frac{W_p}{L_p} \frac{(V_I - Vdd - V_{Tp})^2}{2}. \tag{2.25}$$

Again using the assumption of equation 2.23, this expression can also be reduced and rearranged, yielding the form:

$$V_{IH} = \frac{5Vdd + 5V_{TP} + 3V_{TN}}{8}. \tag{2.26}$$

The noise margins of an NMOS inverter can be found using similar methods. The derivations are not shown here but the steps are identified. Beginning with V_{IH} and examining through graphical techniques the output characteristics, the NMOS inverter is found to be equivalent to the CMOS case; that is, the driver (enhancement mode) is in the linear regime and the load (depletion mode) is in the saturation regime. Assuming that the inverter pull-up: pull-down ratio is k, then:

$$V_{IH} = V_{TN} - \frac{2V_{TD}}{\sqrt{3k}}. \tag{2.27}$$

Considering the NMOS V_{IL}, the driver and load bias regimes are exchanged (as in CMOS), and the result is as follows:

$$V_{IL} = V_{TN} - \frac{V_{TD}}{\sqrt{k(1+k)}}. \tag{2.28}$$

Note that the NM_H of NMOS and CMOS inverters are similar since both achieve $V_{OH} \approx Vdd$. Because an NMOS inverter V_{OL} is not zero (100 mV – 500 mV are typical values), however, the NM_L of NMOS is considerably lower than for a CMOS inverter.

Bibliography

Chen, W.K. (2000). *The VLSI handbook.* CRC Press.

Geiger, R.L., Allen, P.E., and Strader, N.R. (1990). *VLSI design techniques for analog and digital circuits.* New York: McGraw-Hill.

Laker, K.R., and Sansen, W.M.C. (1994). *Design of analog integrated circuits and systems.* New York: McGraw-Hill.

Tsividis, Y. (1996). *Mixed analog-digital VLSI devices and technology: An introduction.* New York: McGraw-Hill.

Vyemura, J.P. (1988). *Fundamentals of MOS digital integrated circuits.* Reading, MA: Addison-Wesley.