II

ELECTRONICS

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With the emergence of digital information age, there is an ever increasing need to integrate various technologies to efficiently perform advanced communication, computing, and information processing functions. Efficient generation and utilization of electric energy is of paramount importance in an energy and environmentally conscious society. This section deals with recent developments in these areas with relevant background information.

In Chapter 1, an account of voltage regulation modules (VRMs) used in powering microchips is provided with a particular emphasis on circuit switching topologies. Chapter 2 deals with noise in mixed-signal electronic systems with a focus on submicron ultra-large scale integrated (ULSI) system-on-a-chip (SOC) technologies. Noise in semiconductor devices and passive components becomes a key issue in addressing system-level signal integrity concerns. A detailed review and progress on metal-oxide-silicon field-effect transistors (MOSFETs) is discussed in Chapter 3 with emphasis on important performance and reliability degradation parameters. These devices form the basic electronic building blocks in a majority of microsystems.

Filters are used in a variety of signal processing circuits. Chapter 4 provides an account of latest advances in the design and application of active filters in microsystems. Although bipolar junction transistors (BJTs) are not as prominent as MOSFETs, nevertheless they are used in a variety of mixed-signal and poweer circuits. Chapter 5 discusses the state-of-the-art on diodes and BJTs in these circuits. Chapter 6 provides insight into basic semiconductor material physics and how it relates to device performance and reliability. The section concludes with a detailed account of the evolution and current state-of-the-art of power semiconductor devices for discrete as well as integrated applications. Power semiconductor devices are playing an increasingly important role in microsystems, especially for performing the power management function.

1

Investigation of Power Management Issues for Future Generation Microprocessors*

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1.1 Introduction

Advances in microprocessor technology pose new challenges for supplying power to these devices. The evolution of microprocessors began when the high-performance Pentium processor was driven by a nonstandard power supply of less than 5 V instead of drawing its power from the 5-V plane on the motherboard (Goodfellow and Weiss, 1997).

Low-voltage power management issues are becoming increasingly critical in state-of-the-art computing systems. The current generation of high-speed CMOS processors (e.g., Alpha, Pentium, and Power PC) operate at above 300 MHz with 2.5- to 3.3-V output voltage. Future processors will be designed with even lower logic voltages of 1 to 1.5 V and increases in current demands from 13 A to 50 to 100 A (Zhang *et al.*, 1996). Meanwhile, operating frequencies will increase to above 1 GHz. These demands, in turn, require special power supplies, voltage regulator modules (VRMs), to provide lower voltages with higher current capabilities for microprocessors. Table 1.1 shows the specifications for present and future VRMs.

As the speed of the processors increases, the dynamic loading of the VRMs is also significantly increased. Future microprocessors are expected to exhibit higher current slew rates of up to 5 A/ns. These slew rates represent a severe problem for the large load changes that are encountered when systems transfer from the sleep mode to the active mode and vice versa. In these cases, the parasitic impedance of the power supply connection to the load and the equivalent series resistor (ESR) and equivalent series inductor (ESL) of the capacitors have a dramatic effect on VRM voltage (Zhang *et al.*, 1996). If this impedance is not low enough, the supply voltage may fall out of the required range during the transient period. Moreover, the total voltage tolerance will be much

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TABLE 1.1 Specifications for Present and Future VRMs

Voltage/Current	Present	Future
Output voltage	2.1 ~ 3.5 V	1 ~ 1.5 V
Load current	0.3 ~ 13 A	1 ~ 50 A
Output voltage tolerance	± 5%	± 2%
Current slew at decoupling capacitors	1 A/nS*	5 A/ns

* Current slew rate at today's VRM output is 30 MS (1997).

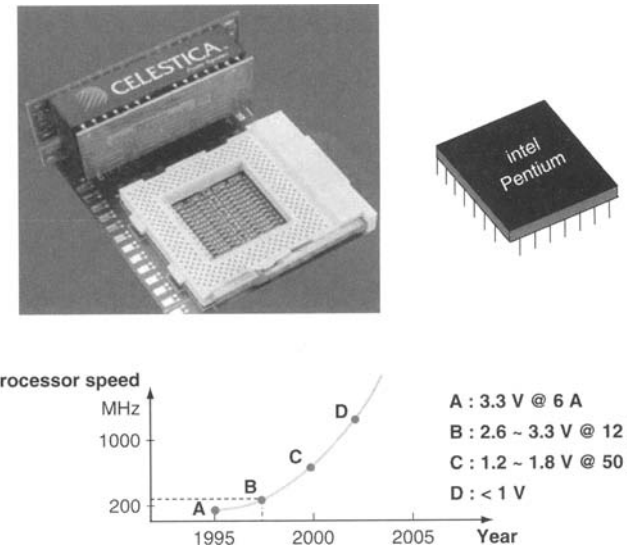


FIGURE 1.1 Today's VRM and Processor Road Map

tighter. Currently, the voltage tolerance is 5% (for a 3.3 V VRM output with a voltage deviation of ± 165 mV). In the future, the total voltage tolerance will be 2% (for a 1.1 V VRM output with a voltage deviation requirement of only ± 33 mV). All of these requirements pose serious design challenges and require VRMs to have very fast transient responses. Figure 1.1 shows today's VRMs and the road map of microprocessors' development.

Today's VRMs are powered up from the 5-V or 12-V outputs of silver boxes that are used for supplying various parts of the system, such as the memory chips, the video cards, and some sub buses. Future VRMs will be required to provide lower voltages and higher currents with tighter voltage regulations. The traditional centralized power system, the silver box, will no longer meet the stringent requirements for VRM voltage regulation because of the distributed impedance associated with a long power bus and the parasitic ringing due to high-frequency operation. On the other hand, with much heavier loads in the future, the bus loss becomes significant. To maintain system stability, a huge silverbox output capacitance is also needed. At the same time, to avoid the interaction between different outputs, a very large VRM input filter capacitance is required. Figure 1.2 shows the trend of computer power system architecture. In the future, a distributed power system (DPS) with a high-voltage bus, 12 V or 48 V, can be the solution for servers' and workstations' power systems. High-performance, high-input-voltage VRMs, however, must be developed.

To meet future requirements, a number of critical issues must be addressed. For example, advanced power devices and control technologies are needed for high-efficiency and high-frequency operations. Today's vertical power device technology cannot provide acceptable levels of conversion efficiency at a multimegahertz level due to its high conduction and switching and gate drive losses. This chapter addresses important issues of advanced VRM topologies for fast transient responses and low ripple voltages as well as advanced packaging technologies for improving power density and thermal management. In addition, this discussion covers the limitations of today's tech-

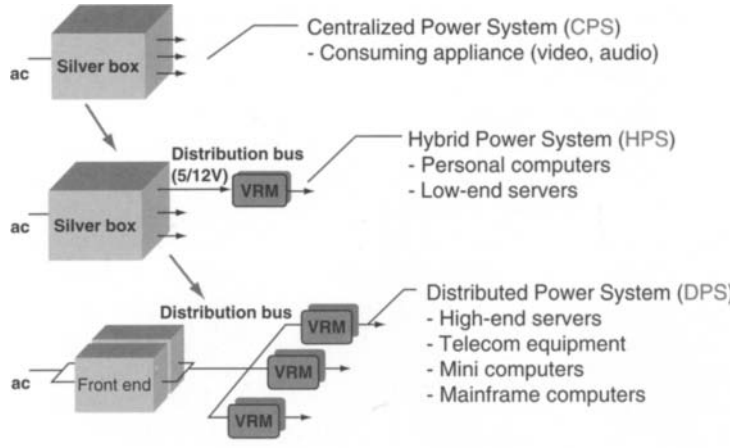


FIGURE 1.2 The Trend of Computer Power System Architecture

nologies, including VRM topologies, power devices, and power systems.

1.2 Limitations of Today's Technologies

1.2.1 Limitations of Present VRM Topologies

Most of today's VRMs use **conventional buck** or **synchronous rectifier buck topologies**. Figure 1.3 shows the conventional buck circuit, which is the most cost-effective approach. Usually, Schottky diodes are used as rectifiers. The top metal-oxide-semiconductor field effect transitor (MOSFET) transfers energy from the input, and the bottom rectifier conducts the inductor current. The control regulates the output voltage by modulating the conduction interval at the top MOSFET. Figure 1.4 shows the synchronous rectifier buck circuit. This topology increases the efficiency by replacing the rectifier with a low Rds(on) MOSFET. The synchronous switch is controlled by the complementary signal of the top switch's gate signal. The synchronous rectifier buck always operates in continuous current mode. Its transient response is faster than that of a conventional buck converter. Conventional VRMs use large output filter inductances, $2 \sim 4\ \mu H$, to reduce ripple.

Figure 1.5 shows the practical VRM load model (processor model). The packaging capacitor is the parasitic capacitor inside the microprocessor package. There are several decoupling capacitors near and around the microprocessors to reduce noise and maintain voltage regulation. Bulk capacitors are VRM output capacitors. In very high-speed and high-current systems, physical capacitors can no longer be simplified as ideal capacitors. The parasitic parameters play very important roles. The capacitor should be considered as an ideal capacitor in series with an ESR and an ESL, as shown in Figure 1.6 (Wong, 1997).

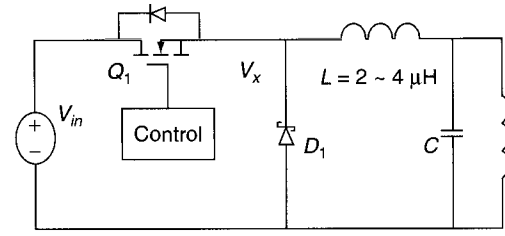


FIGURE 1.3 Conventional Buck Converter

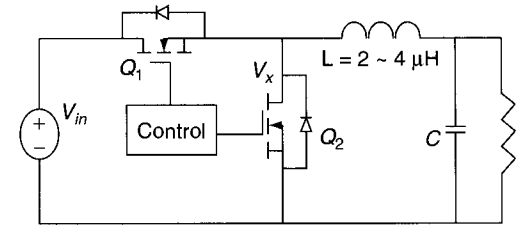


FIGURE 1.4 Synchronous Rectifier Buck Converter

There are interconnection parasitic inductances and resistances between bulk capacitors and decoupling capacitors and between decoupling capacitors and packaging capacitors. Future microprocessor load transitions will have a 5-A/ns slew rate. In this case, all these parasitics have a significant

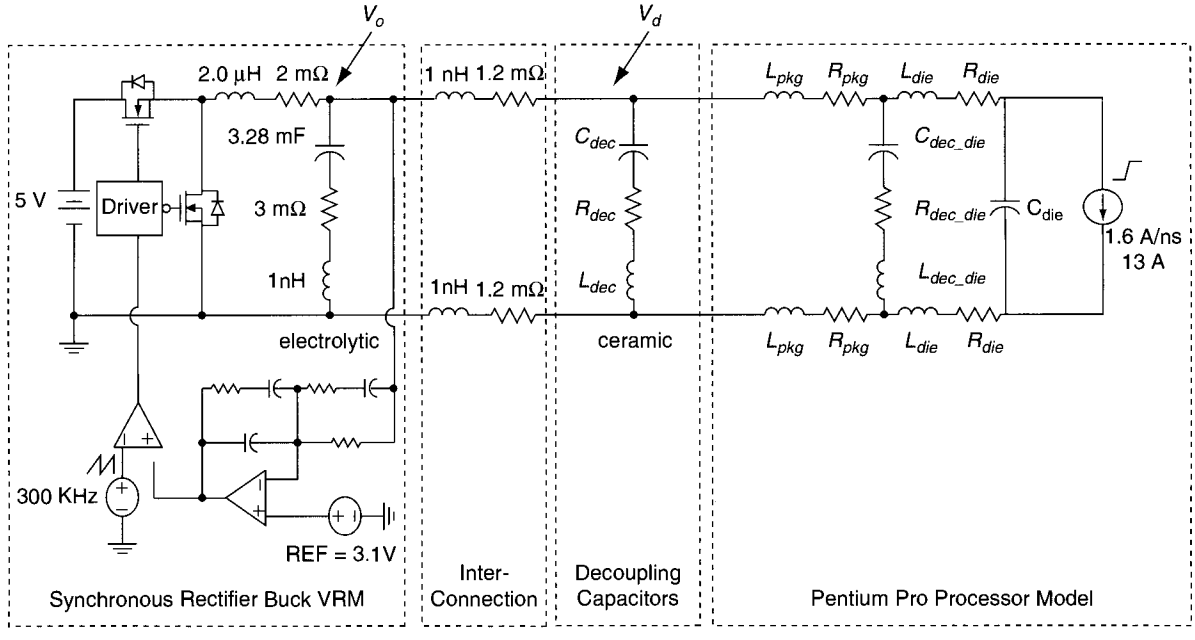


FIGURE 1.5 Practical VRM Load: Pentium Pro Processor Model

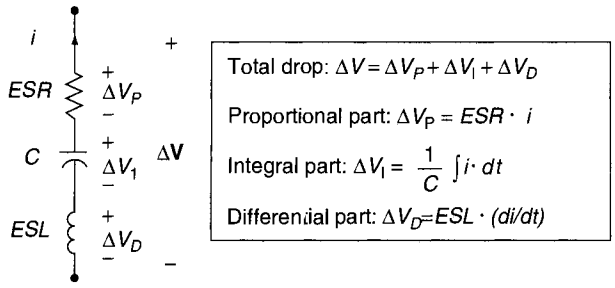


FIGURE 1.6 The Voltage Drop of a Capacitor Divided into Three Parts: Proportional, Integral, and Differential

effect on the VRM transient voltage. Figure 1.7 shows the transient response of a synchronous rectifier VRM. The VRM's input voltage is 5 V, and its load changes from 0.8 A to 30 A. It is obvious that for future microprocessor loads, today's VRM topologies cannot meet the 2% transient requirement.

During the transient, there are three spikes in the voltage drop (Wong, 1997). The first high-frequency spike is dominated by loop 1, shown in Figure 1.8, which combines the parasitic of the packaging capacitors and decoupling capacitors and the interconnection between them. The second spike is controlled by loop 2, which combines the parasitic of the decoupling capacitors and VRM bulk capacitors and the interconnection between them. The third spike is decided by loop 3, which combines the parasitic of the VRM output filter inductor and the VRM output bulk capacitors.

The transient limitation of today's VRM topologies comes from their large output filter inductance. During the transient, this large inductor limits the energy transfer speed so that the capacitors have to store or discharge all the energy from the load. For future microprocessors, because of heavier load currents, higher load transient slew rates, and tighter voltage tolerance requirements, more decoupling capacitors will be required to reduce the second spike, and more VRM output bulk capacitors will be required to reduce the third spike. As a result, to meet future specifications, 23 times the decoupling capacitors will be needed, and 3 times VRM bulk capacitors will be needed (Wong, 1997). The VRM will be very large and expensive. The space of the VRM, however, is limited and the real estate of the motherboard is expensive. The need for a large quantity of capacitors makes VRMs, which use these topologies, impractical for future microprocessors.

1.2.2 Limitations from Power Devices

Another limitation of today's VRMs is efficiency. Figure 1.9 shows the conventional VRM efficiency at a 2-V output. Using IRL3803 as switches, with an on-resistance of 6 mΩ and a 30-V

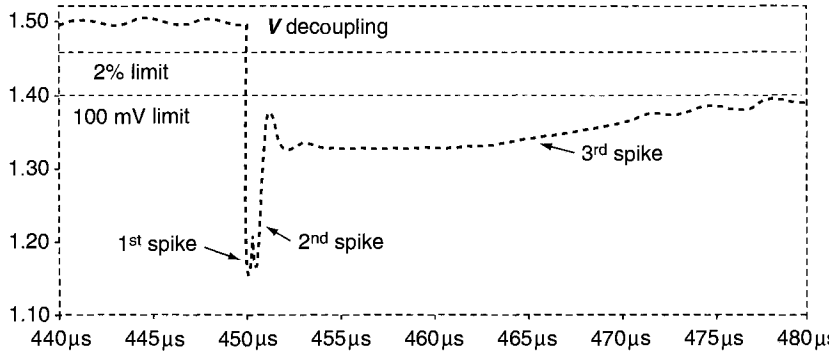


FIGURE 1.7 Transient Response of Conventional VRMs (V_{in} = 5 V, load: 0.8 A to 30 A, and fs = 300 kHz)

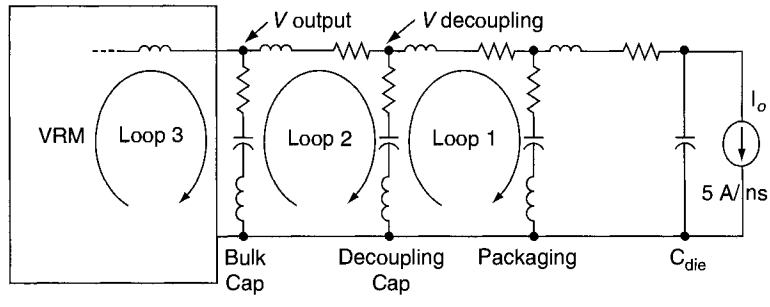


FIGURE 1.8 The Processor Model: Three Resonant Loops with Different Resonant Frequencies

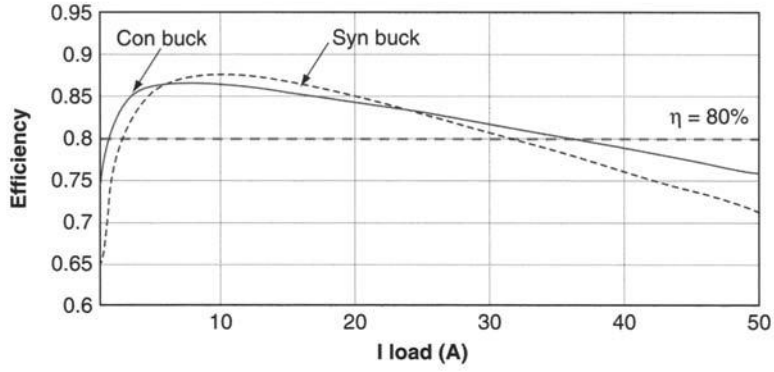


FIGURE 1.9 Conventional VRM Efficiency
($V_{in} = 5\,V$, $V_o = 2\,V$, $fs = 300$ kHz, and switches: IRL3803)

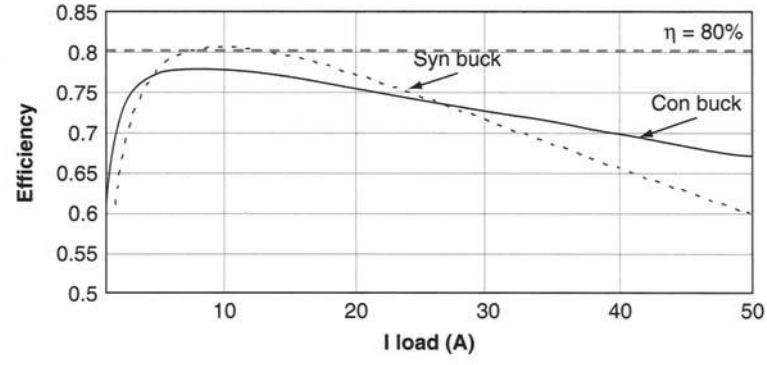


FIGURE 1.10 Conventional VRM Efficiency
($V_{in} = 5\,V$, $V_o = 1.2\,V$, $fs = 300$ kHz, and switches: IRL3803)

voltage rating, the conventional VRM cannot meet the 80% efficiency requirement at heavy load. For lower output voltages, it will be even more difficult to meet the efficiency requirement. Figure 1.10 shows the conventional VRMs' efficiency at a 1.2-V output. Their efficiency is lower than 80% in the whole load range.

This limitation stems from today's power devices' technology. Based on vertical power MOSFET technology, most of today's low-voltage power MOSFETs are available at a rating of 30 V. Roughly, the total power loss of a power device can be divided into three parts: conduction loss, gate drive loss, and switching loss. Figure 1.11 shows the relationship between conduction loss, gate drive loss, and switching loss. For this kind of low-voltage, high-current application, conduction loss contributes a large percentage of the total loss. When only one IRL3803 is used, the MOSFET's conduction loss is 25 times the gate drive loss plus the switching loss. To reduce conduction and total loss, more switches need to be paralleled. This does not necessarily mean, however, that more parallel switches equals lower total loss. When five IRL3803 are paralleled, the total loss is reduced to the minimum. After this point, adding more switches will not improve efficiency. Figure 1.12 shows the number of parallel

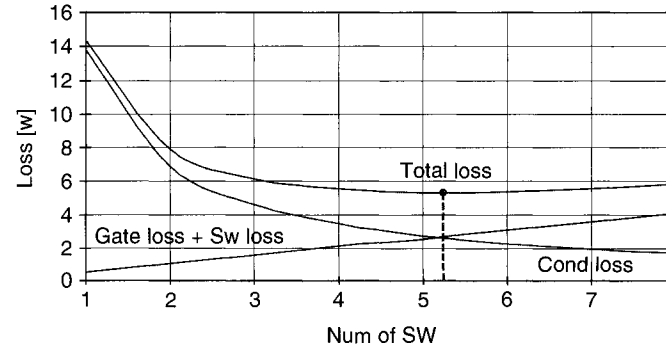


FIGURE 1.11 Switching Loss, Gate Drive Loss, and Conduction Loss of an IRL3803 Versus a Parallel Switch Number
($V_{in} = 5\,V$, $fs = 300$ kHz, and I load $= 50\,A$)

switches needed to meet the 80% efficiency requirement when the input voltage is 5 V. In Figure 1.12 (A), when the output voltage is 2 V, paralleling two switches can enable the device to meet the efficiency requirement at heavy load. However, when the output voltage is 1.2 V, as shown in Figure 1.12 (B), no matter how many switches are in parallel, the VRM cannot meet the 80% efficiency requirement at heavy

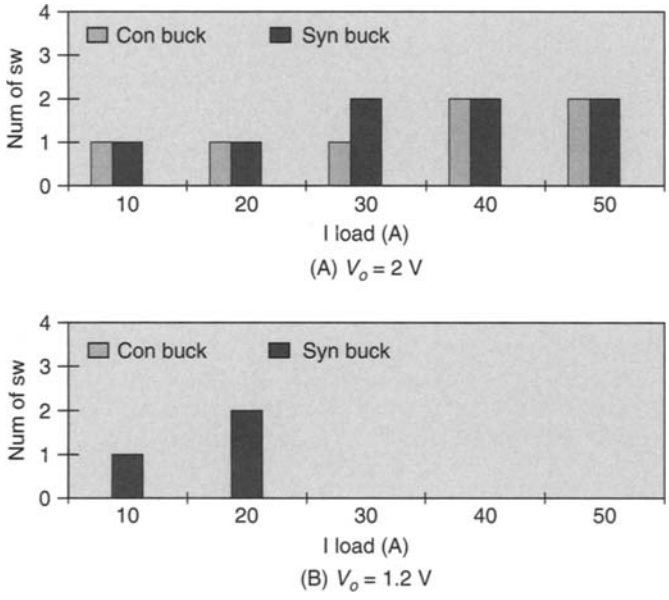


FIGURE 1.12 The Number of Parallel Switches Needed to Meet the Efficiency Requirement
(V_{in} = 5 V, fs = 300 kHz, and efficiency >80%)

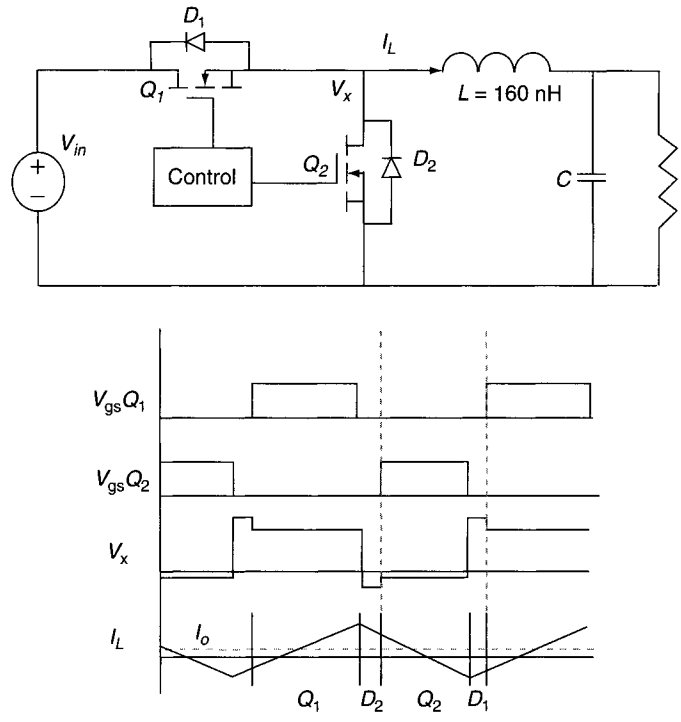


FIGURE 1.13 Quasi-Square-Wave (QSW) VRM Topology

load (>30). This limitation is due to the high figure of merit (FOM) of today's devices. The FOM is equal to Rds(on) times gate charge (Qg). For today's device technology, the lowest FOM value is around 300(mΩ × nC). With such a high FOM value, power devices not only limit the VRM's efficiency but also limit the VRM's ability to operate at higher operating frequencies. Most of today's VRMs operate at a switching frequency lower than 300 kHz. This low switching frequency causes slow transient responses and creates a need for very large energy storage components.

1.3 Advanced VRM Topologies

1.3.1 Low-Input-Voltage VRM Topologies

A Fast VRM Topology: The Quasi-Square-Wave (QSW) VRM

To overcome the transient limitation occurring in conventional VRMs, a smaller output filter inductance is the most desirable option for increasing the energy transfer speed. Figure 1.13 shows the quasi-square-wave (QSW) circuit. The QSW topology keeps the VRM output inductor current touching zero in both sleep and active modes. When Q_1 turns on, the inductor current is charged to positive by the input voltage. After Q_1 turns off and before Q_2 turns on, the inductor current flows through Q_2's body diode. When Q_2 turns on, the inductor current is discharged to negative. After Q_2 turns off and before Q_1 turns on, the inductor current flows through Q_1's body diode. Compared with conventional buck and synchronous buck topologies, the output filter inductance is reduced significantly. At a 13-A load and a 300-kHz switching frequency, the QSW circuit needs only a 160-nH inductor, as compared with the 2 ~ 4 μH inductor needed in the conventional design. This small inductance makes the VRM transient response much faster. Figure 1.14 shows the transient response of the QSW topology. The third spike of the output voltage becomes insignificant, and the second spike is reduced significantly.

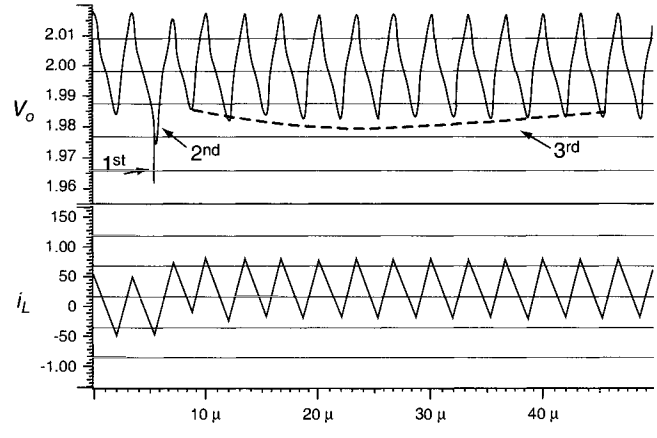


FIGURE 1.14 Transient Response of the QSW

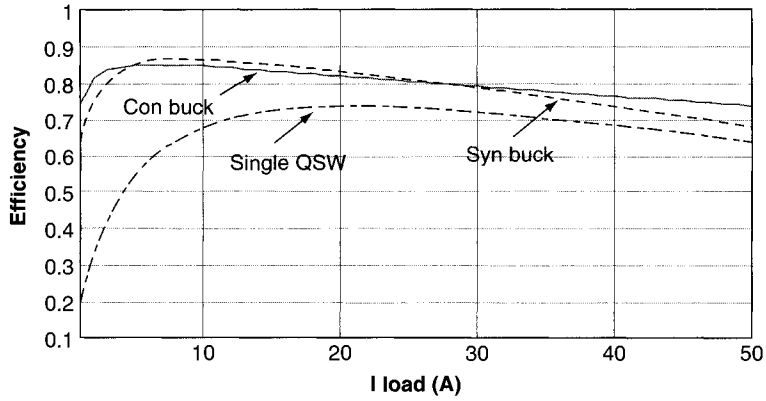


FIGURE 1.15 Efficiency of the QSW Compared with a Conventional VRM ($V_{in} = 5\,V$, $V_o = 2\,V$, and $fs = 300$ kHz)

There are two disadvantages to this fast VRM topology. The first one is the large current ripple. A huge VRM output filter capacitance is needed to suppress the steady-state ripple. The smaller inductance results in a faster transient response but requires a larger bulk capacitance. The second disadvantage is its low efficiency. In Figure 1.15, due to the large ripple current, the QSW switch has a larger conduction loss. Its efficiency is lower than that of a conventional VRM.

A Fast VRM with a Small Ripple: The Interleaved QSW VRM

To meet both the steady state and transient requirements, a novel VRM topology, the interleaved QSW, is introduced in Figure 1.16. The interleaved QSW topology naturally cancels the output current ripple and still maintains the fast transient response characteristics of the QSW topology. A smaller capacitance is needed compared to both the single-module QSW VRM and the conventional VRM. The more modules in parallel, the better the ripple canceling effect. Figure 1.17 shows a four-module interleaved QSW VRM. Figure 1.18 shows its transient response. The results show that this technique can meet future transient requirements without a large steady-state voltage ripple. Compared with the single-module QSW topology, the efficiency is improved significantly. Figure 1.19 shows the efficiency comparison results.

Figure 1.20 shows a four-module interleaved QSW VRM prototype picture. In the VRM, an integrated magnetic design is used. Every two inductors use one magnetic core. As a result, in total, two magnetic cores are used for these four channel inductors. Figure 1.21 shows the integrated magnetic structure (Chen 1999). By taking advantage of the interleaving technology, the AC flux of the two inductors is canceled out in the center leg. As a result, the core loss and center leg crossing area are reduced. The planar core structure

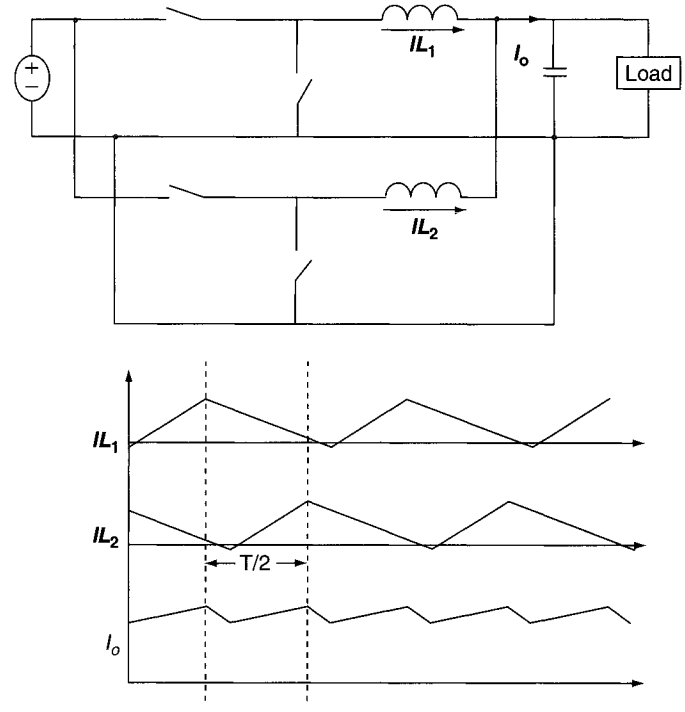


FIGURE 1.16 Current Ripple Cancelling Effect of Interleaved QSW

makes a very low-profile VRM. This kind of low-profile magnetic also has good thermal management. In the magnetic design, the PCB trace is used as the inductor winding. This approach is very cost-effective. In addition, the termination loss is eliminated.

Table 1.2 compares the four-module interleaved QSW VRM design with the conventional VRM. Since the necessary capacitance is reduced, the VRM power density is dramatically increased by six times. Also, since each module handles a lower current, the circuit will be packaged more easily. The test results in Figure 1.22 show the transient response of the

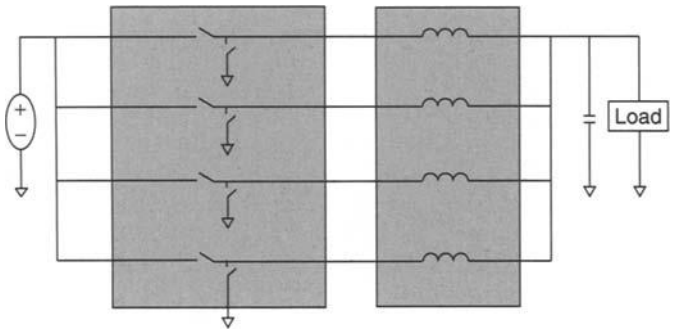


FIGURE 1.17 A Four-Module Interleaved QSW VRM

four-module interleaved QSW VRM compared to today's commercial VRM. The interleaved QSW topology can not only reduce output current ripple, but it can also reduce input current ripple.

1.3.2 High-Input-Voltage VRM Topologies

Most of today's VRMs draw power from the 5-V output of the silver box. This bus voltage is too low for future low-voltage, high-current processors' applications. A distributed power system (DPS) with a high bus voltage can be the solution for future computer systems, such as servers' and workstations' power systems. In a high-voltage bus-distributed system, the bus conduction loss is lower and the distribution bus is easy to

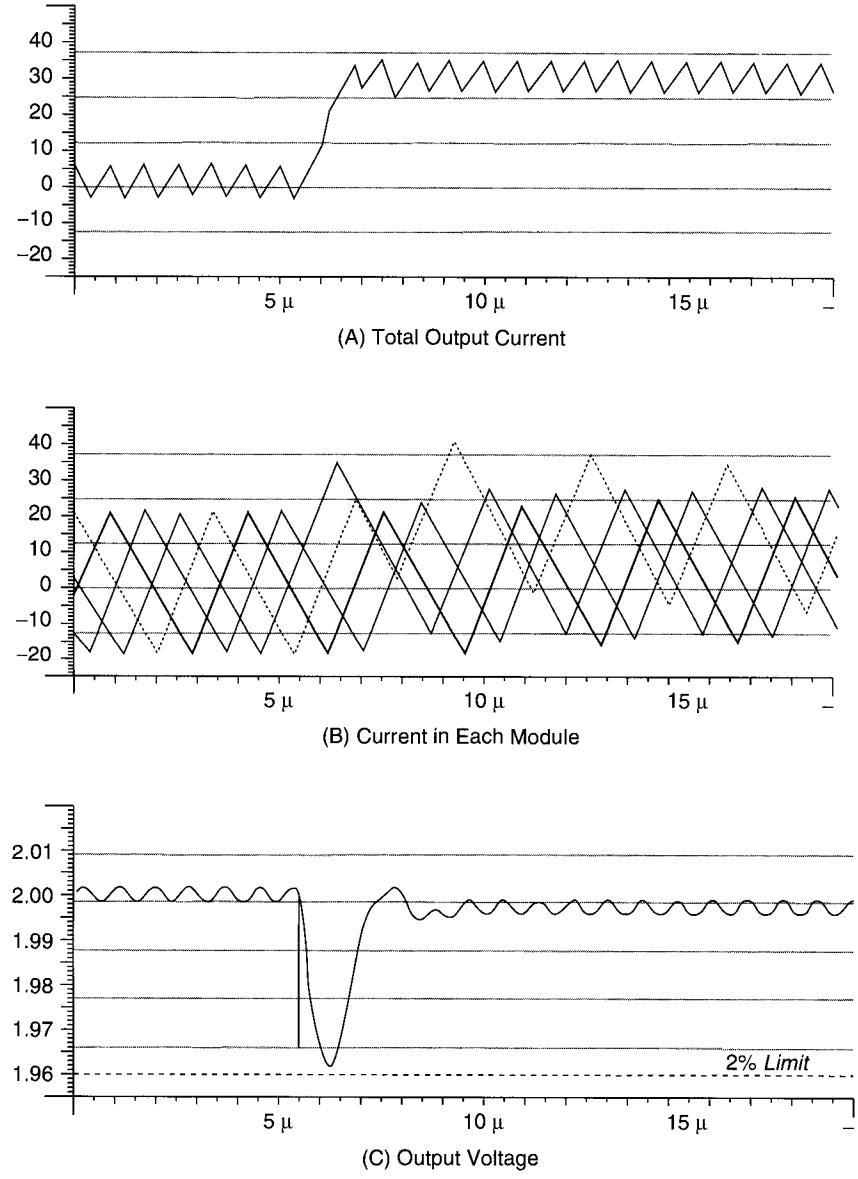


FIGURE 1.18 Transient Response of the Four-Module Interleaved QSW

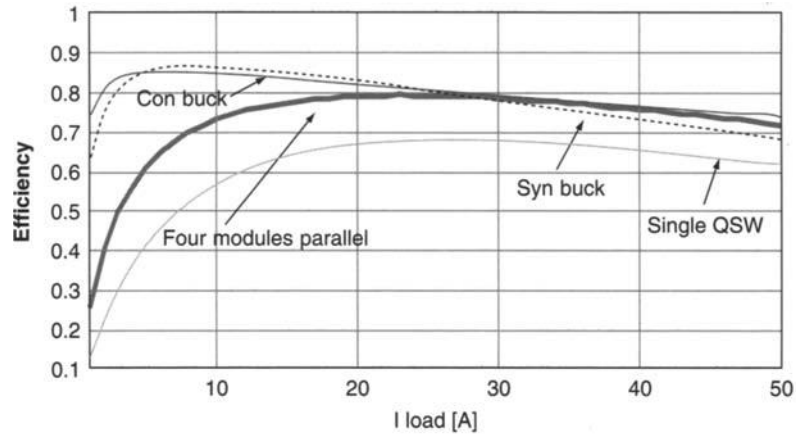


FIGURE 1.19 Efficiency Comparison

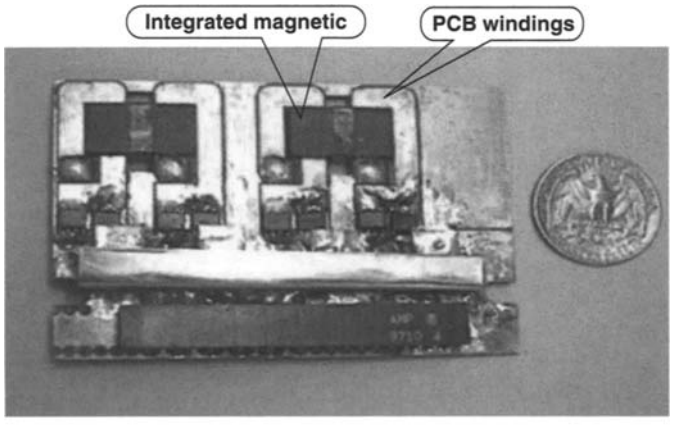


FIGURE 1.20 The Four-Module Interleaved QSW VRM

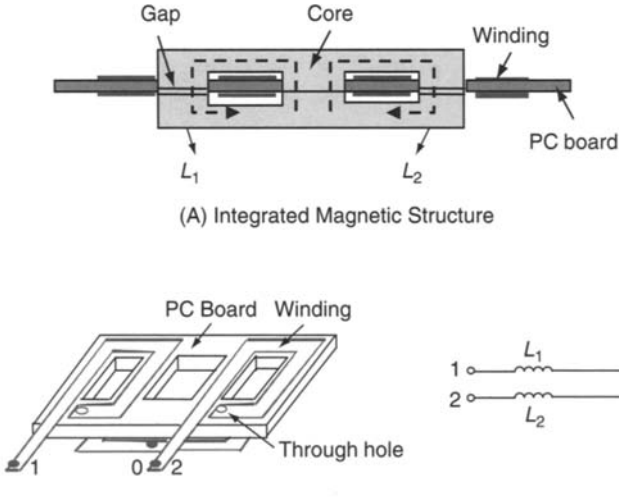


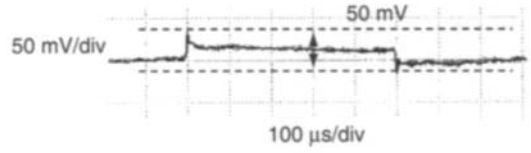
FIGURE 1.21 Integrated Magnetic Structure

TABLE 1.2 Design Comparison of the Interleaved QSW VRM and the Conventional VRM

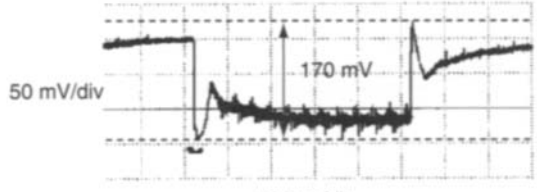
	Interleaved QSW	Conventional VRM
V_{in}	5	5
Bulk capacitance	1200 μF	8000 μF
Output inductance	320 nH (×4)	3.8 μH
Transient voltage drop:	50 mV	150 mV
V_o @ load	2 V@30 A	2 V@13 A
Power-stage-power density (W/in^3)	30	3 ~ 5

design. On the other hand, in this kind of system, the transient of the load-end converter will have less effect on the bus voltage and thus less effect on the other load-end converters. As a result, for future applications, the high-input-voltage VRMs' input filter size can be dramatically reduced. Figure 1.23 shows the results. When the bus voltage increases from 5 V to 48 V, the VRM input filter capacitance can be reduced from 10 mF to 10 μF.

For high-voltage bus systems, advanced high-input-voltage VRM topologies must be developed. For example, if the buck converter shown in Figure 1.3 is used in a high-voltage bus system, the VRM's duty cycle is very asymmetrical. When the input voltage is 12 V and the output voltage is 2 V, the VRM duty cycle is only 0.16. Figure 1.24 shows the asymmetrical transient response of a synchronous buck VRM. When the load changes from a light load to a heavy load, since the inductor charging voltage $(V_{in} - V_o)$ is high, the VRM's step-down voltage drop is small. When the load changes from a heavy load to a light load, since the inductor discharging voltage V_o, is low, the VRM's step-up voltage drop is large. This asymmetrical transient response makes the output filter overdesigned. Besides, it is difficult to optimize efficiency in an asymmetrical duty cycle converter. Figure 1.25 shows the efficiency comparison for different input



(A) Transient Response of the Four-Module Interleaved QSW



(B) Transient Response of the Conventional VRM

FIGURE 1.22 Transient Response Test Results

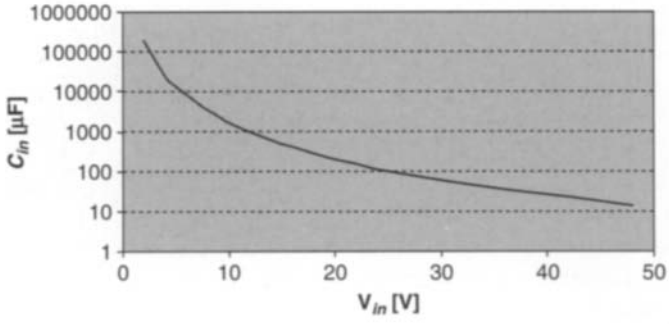


FIGURE 1.23 Input Filter Capacitance Versus Input Voltage

voltages. With a higher input voltage, the VRM has a lower efficiency.

1.3.3 A Nonisolated, High-Input-Voltage VRM Topology: The Center-Tapped Inductor VRM

With advanced inductor designs, the VRM duty cycle can be adjusted. Figure 1.26 shows a changed inductor structure, a center-tapped inductor, that can improve the VRM duty cycle. Figure 1.27 shows an improved VRM topology with the center-tapped inductor structure and a loss-less snubber that can absorb the leakage inductance energy as well as reduce ripple and voltage spikes (Zhou, 1999). With this topology, VRMs do not need high-side gate drives, thus improving VRM efficiency at high-input-voltages. To reduce input and output current ripple, an interleave technique can be used, which is shown in Figure 1.28. Figure 1.29 shows the efficiency of this two-channel interleaved center-tapped inductor VRM efficiency. Its input voltage is 12 V, and its output voltage is 1.2 V. In the test, IRL3103D1 is used as top switch, and two MTP75N03DHs in parallel are used as a synchronous rectifier. This topology can achieve 80% efficiency at 1.2 V at a 60 A output.

1.3.4 An Isolated High-Input-Voltage VRM Topology: The Push-Pull Forward Topology

Another approach to adjusting the VRM duty cycle in high-voltage bus systems is to use transformers. By designing the transformer's turns ratio, VRMs can simply adjust their duty cycles to optimize efficiency and cancel the ripple.

Figure 1.30 shows the push-pull forward VRM topology (Zhou, 1999). In the primary side, switch and transformer windings are alternately connected in a circle. A capacitor is connected between any of two interleaved terminations. The left two terminations are connected to the input and ground, respectively. The two primary windings have the same turns. Figure 1.31 explains the operation of this converter.

Compared with conventional high-input-voltage VRM topologies, the push-pull forward converter has a higher power density, faster transient response, and higher efficiency. For example, compared with the forward flyback shown in Figure 1.32 and asymmetrical half-bridge shown in Figure 1.33, which are fourth-order systems, the push-pull forward converter is a second-order system. Therefore, its control is simpler, and its transient is faster. As a result, the output filter inductance and capacitance needed are significantly reduced. Due to its reduced input current ripple, the converter's input filter can also be reduced.

Compared with half-bridge converters and asymmetrical and symmetrical half-bridge converters, the push-pull forward topology has a larger transformer's turns ratio. For example, if VRM input voltage is 48 V and output voltage is 3.3 V, for both the symmetrical and asymmetrical half-bridges, the transformer's turns ratio is 3 to 1. For the push-pull forward converter, the transformer's turns ratio is 6 to 1. Therefore, the conduction loss of the primary switches in a push-pull forward converter is lower. As a result, the push-pull forward converter has a higher efficiency. At heavy load, the efficiency of the push-pull forward converter is 2 to 3% higher than that of either half-bridge converter.

Figures 1.34(A) and 1.34(B) show the efficiencies of the push-pull forward converter under 12 V and 48 V input voltages, respectively. For a 12-V input, this converter can achieve 81% efficiency at an output of 1.2 V at 60 A. For a 48-V input, this converter can achieve 83.6% efficiency at an output of 1.2 V at 60 A.

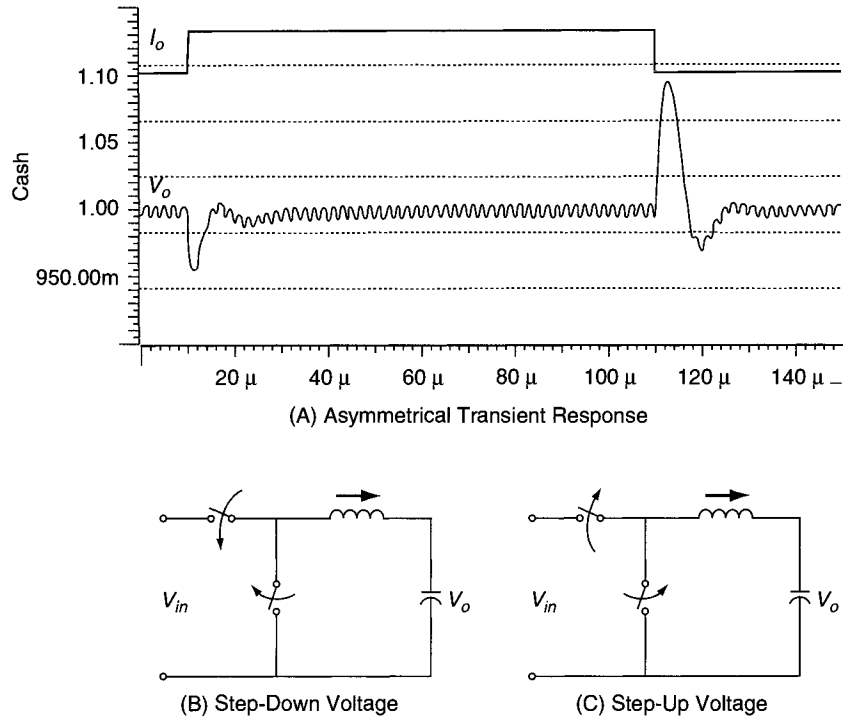


FIGURE 1.24 An Asymmetrical Transient Response from Low-Output-Voltage and High-Input-Voltage

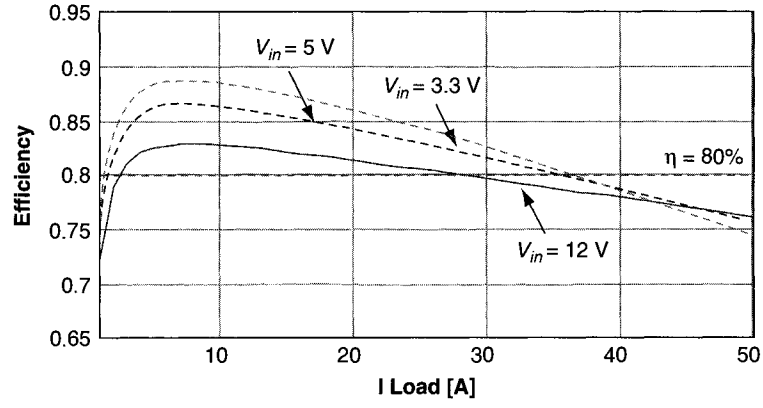


FIGURE 1.25 Efficiency Comparison of Buck Converters ($V_o = 2$ V, $fs = 300$ kHz, and switches: IRL3803)

1.4 Future VRMs

1.4.1 High-Frequency and High-Power-Density *VRMs*

To develop low-cost, high-efficiency, low-profile, high-power density, fast-transient-response, board-mount VRM modules for future generation microprocessor loads, high operating frequencies are desirable. Figure 1.35 shows the transient response of the interleaved QSW VRM when it operates at 1 MHz. Obviously, the voltage spike is reduced significantly. Figure 1.36 shows the inductance and capacitance needed in the interleaved QSW VRM when it operates at a high switching frequency. At 10 MHz, the inductance needed is only 9.25 nH and the capacitance needed is only 5.26 µF. With such a small inductance and capacitance, very high-power-density VRMs can be created, and energy storage costs can be dramatically reduced. Because of today's device technology, however, most VRMs' operating frequencies are lower than 300 kHz. Even at this frequency, the VRM cannot meet efficiency requirements. When the frequency is increased, the resulting VRM efficiency levels are shown in Figure 1.37. At 10 MHz, the VRM will only

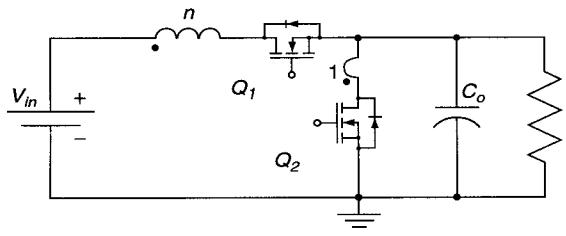


FIGURE 1.26 Center-Tapped Inductor Structure

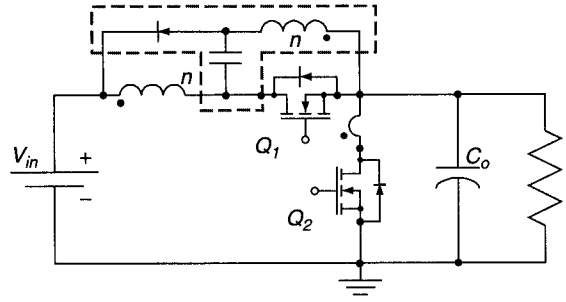


FIGURE 1.27 Improved VRM Topology with a Center-Tapped Inductor and a Lossless Snubber

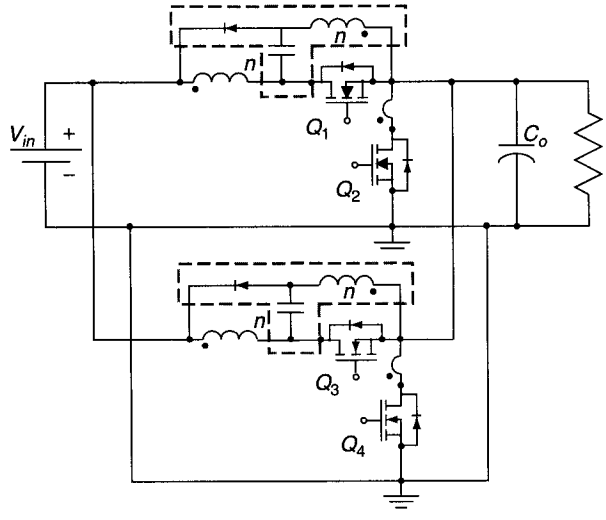


FIGURE 1.28 Interleaved Center-Tapped Inductor VRM

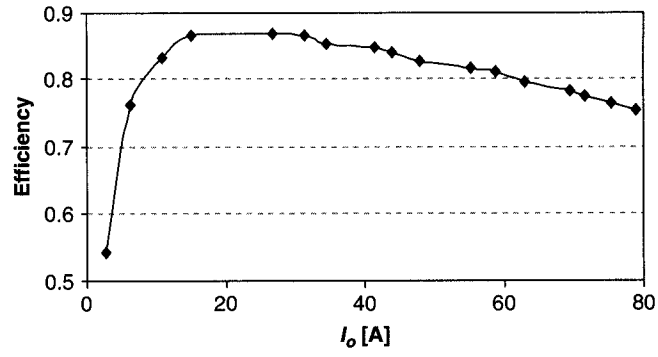


FIGURE 1.29 Efficiency of the Two-Channel Interleaved Center-Tapped Inductor VRM

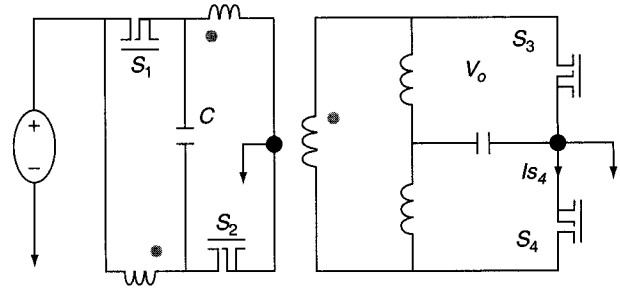


FIGURE 1.30 A Novel Topology: The Push-Pull Forward Converter

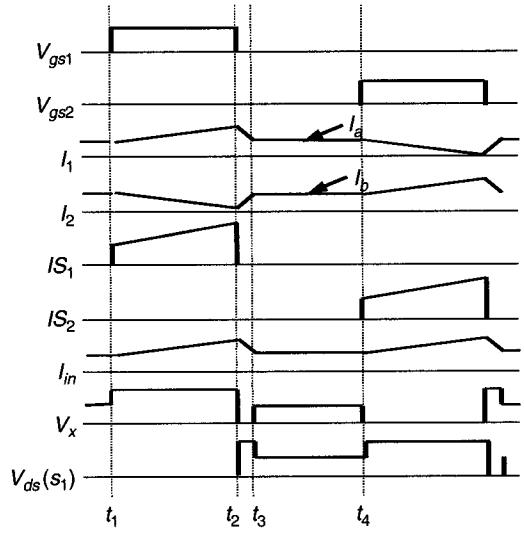


FIGURE 1.31 The Operation of the Push-Pull Forward Converter

have 40% efficiency. This efficiency makes thermal management and packaging very difficult.

For future microprocessor applications, the power device must have a smaller FOM value [$< 100(\text{m}\Omega \times nC)$] and a lower miller charge. With improved device technologies, such as the SOI LDDMOS technology (Huang, 1998), future VRM efficiency will be higher than 90% at several megahertz operating frequencies. Figure 1.38 shows the difference between a vertical DMOS and the proposed LDD MOSFET on SOI structure, whose power density is higher than 100 W/in^3. Table 1.3 shows the VRM efficiency comparison based on today's device technology and the improved LDDMOS technology.

Although advanced topologies have very fast transients, and future device techniques can operate at very high frequencies,

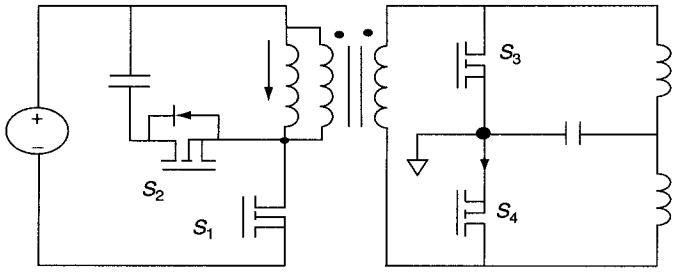


FIGURE 1.32 Flyback Forward Converter

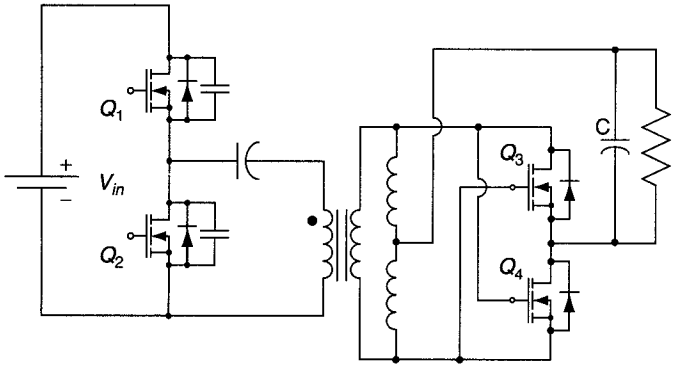


FIGURE 1.33 Asymmetrical Half-Bridge Converter

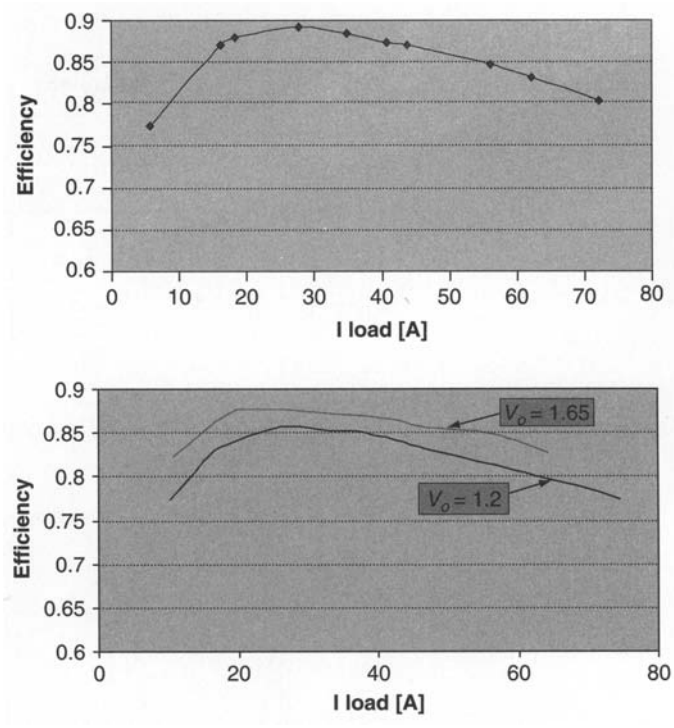


FIGURE 1.34 Push-Pull Forward Efficiency (A) Efficiency of the Push-Pull Forward Converter (V_{in} = 48 V, V_o = 1.2 V, fs = 100 kHz; secondary side uses four MTP75N03DHL, and primary side uses two IRF630). (B) Efficiency of the Push-Pull Forward Converter (V_{in} = 12 V, fs = 100 kHz; secondary side uses four MTP75N03DHL, and primary side uses two IRL3103D1).

to minimize the effects of the interconnections an innovative design with a possible integration of the VRM and the processor is still the key to meeting the ever-increasing demand for processor performance and speed.

The integration of the VRM with the processor can take either a hybrid or a monolithic approach. In the hybrid approach, the VRM can be made as a silicon chip with all the control functions. Figure 1.39 shows an integration-packaging example. As shown in Figure 1.39(A) and (B), several VRM chips can be placed in parallel and be mounted close to the microprocessor on the same cartridge. Ceramic capacitors with small ESRs and ESLs can be used as the output capacitors and can be placed on the PCB board next to the processor. By connecting the output of the VRM and the power input of the processor via a path through a magnetic material sheet, the small output inductor can also be created. With this kind of packaging approach, interconnection parasitics can be minimized. For future applications, some other advanced packaging technologies, such as flip-chip technology, can also be used.

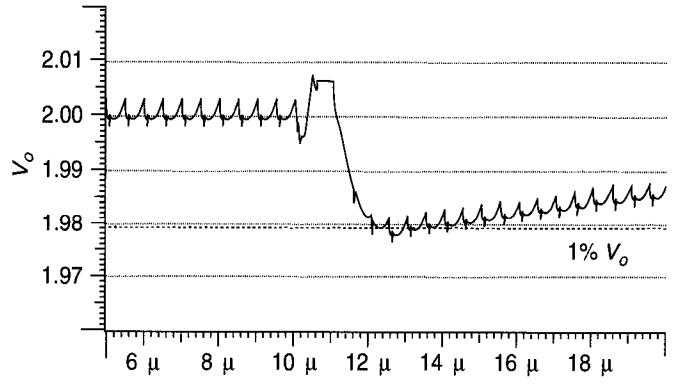
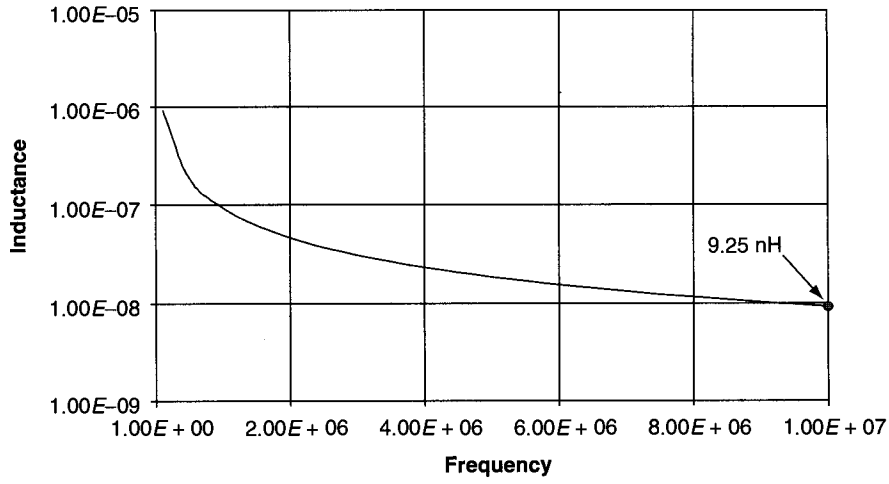
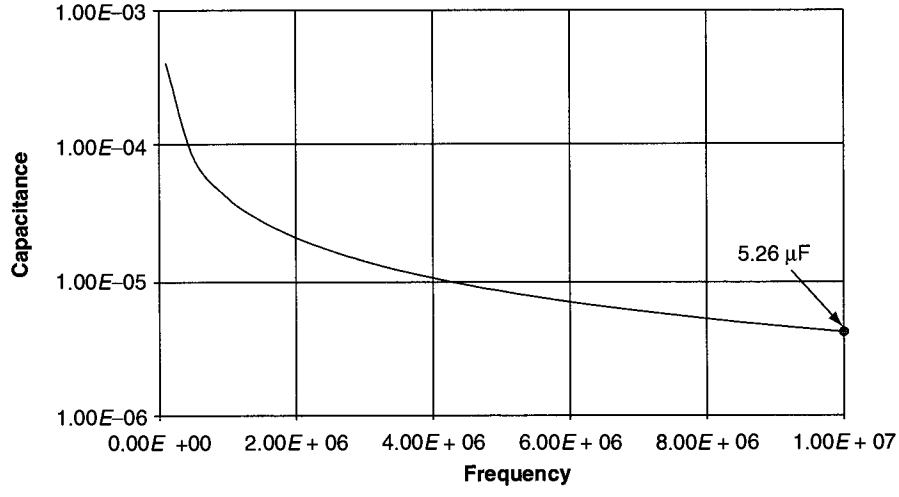


FIGURE 1.35 Transient Response of the Interleaved QSW (V_{in} = 5 V, V_o = 2 V, and fs = 1 *MHz*)



(A) Inductance Needed Versus Frequency



(B) Capacitance Needed Versus Frequency

FIGURE 1.36 Inductance and Capacitance Needed in the Interleaved QSW VRM Topology at a High Operating Frequency

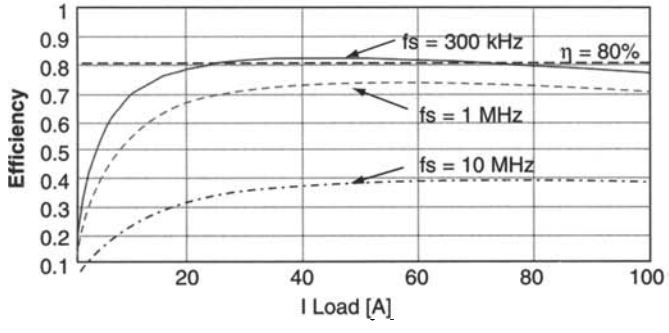


FIGURE 1.37 VRM Efficiency Based on Today's Device Technology ($V_{in} = 5\,V$, $V_o = 2\,V$, and Switches 5 IRL3803 in parallel)

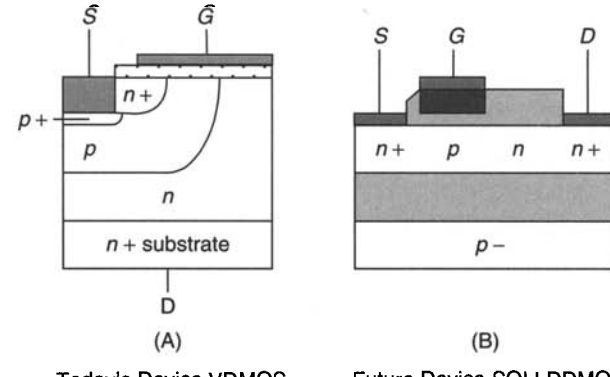


FIGURE 1.38 Future Power Device Technology

TABLE 1.3 VRM Efficiency Comparisons

$V_{in} = 5V$ $V_o = 2V$	BV [V]	FOM [mΩ · nC]	Optimized efficiency for interleaved QSW VRM		
			300 kHz	1 MHz	10 MHz
LDDMOS	10	77	95%	91%	88%
Today's device	30	473	87%	79%	60%

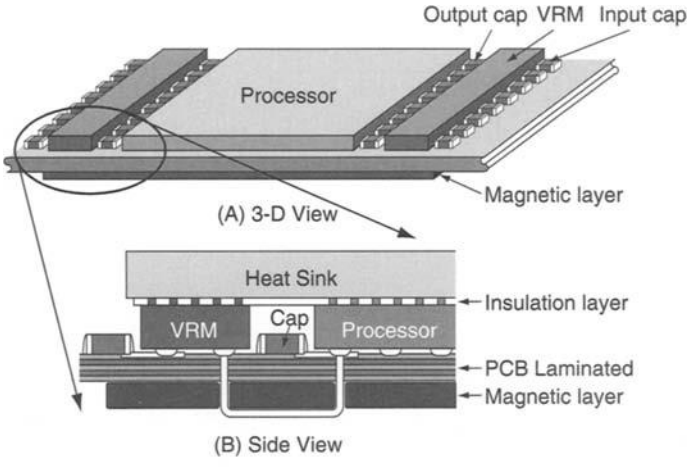


FIGURE 1.39 Hybrid Approach

1.5 Conclusions

For future microprocessor applications, there are many power management issues that need to be addressed, such as those concerning VRM topologies, power device technologies, and packaging technologies. To meet future requirements, VRMs should have high-power densities, high efficiencies, and fast transient performances. To achieve this target, advanced VRM topologies, advanced power devices, and advanced packaging technologies must be developed.

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